AMENDMENTS TO THE CLAIMS

Please cancel claims 2-3, 13-14, and 19-22 without prejudice. Kindly amend claims 1, 4, 6, 10, and 15 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A multiple mode clock receiver, comprising:

first and second input AC-coupled capacitors, wherein said first and second input AC-coupled capacitors comprise first and second N-channel devices, respectively, each having a source and a drain coupled together at respective input and a gate coupled to a corresponding one of a first junction and a second junction;

a first voltage divider coupled between DC source voltages and ~~having a~~ having said first junction coupled to said first input AC-coupled capacitor;

a second voltage divider coupled between DC source voltages and ~~having a~~ having said second junction coupled to said second AC-coupled ~~capacitor; and~~capacitor;

a differential amplifier, having a differential input including a first input coupled to said first junction and a second input coupled to said second junction, and having an output;

a third N-channel device having a source coupled to said source of said first N-channel device and a drain and a gate coupled to said first junction; and

a fourth N-channel device having a source coupled to said source of said second N-channel device and a drain and a gate coupled to said second junction;

wherein said output of said differential amplifier provides an output clock signal that is aligned with an input clock signal provided through at least one of said first and second input AC-coupled capacitors.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The multiple mode clock receiver of claim 3, wherein said third and fourth N-channel devices are provided to stabilize said differential amplifier in the event of clock shutdown~~each comprise relatively weak devices~~.

5. (Currently Amended) The multiple mode clock receiver ~~of claim 2~~of claim 1, wherein said first and second voltage dividers each comprise:

a first P-channel device having a source and a substrate coupled to a source voltage and a gate and a drain coupled to a corresponding one of said first and second junctions; and

a second P-channel device having a source and gate coupled to ground and a drain and a substrate coupled to a corresponding one of said first and second junctions.

6. (Currently Amended) The multiple mode clock receiver of claim 5, wherein said first and second N-channel devices are sized ~~sufficiently large~~ to overcome parasitic capacitances of said first and second P-channel devices.

7. (Original) The multiple mode clock receiver of claim 5, wherein said first P-channel device of said first voltage divider is matched with said first P-channel device of said second voltage divider, and wherein said second P-channel device of said first voltage divider is matched with said second P-channel device of said second voltage divider.

8. (Original) The multiple mode clock receiver of claim 5, wherein said differential amplifier comprises:

a fifth P-channel device having a source and a substrate coupled to a voltage source, a gate coupled to a center node and a drain;

a sixth P-channel device having a source and a substrate coupled to said voltage source, and a gate and drain coupled together at said center node;

a third N-channel device having a source, a gate coupled to said first junction, and a drain coupled to said drain of said fifth P-channel device;

a fourth N-channel device having a drain coupled to said source of said third N-channel device, a gate coupled to said center node, and a source coupled to ground;

a fifth N-channel device having a source coupled to said source of said third N-channel device, a gate coupled to said second junction, and a drain coupled to said drain of said sixth P-channel device; and

a sixth N-channel device having a drain coupled to said source of said fifth N-channel device, a gate coupled to said center node, and a source coupled to ground.

9. (Original) The multiple mode clock receiver of claim 8, further comprising an inverter having an input coupled to said drain of said fifth P-channel device and an output providing said output clock signal.

10. (Currently Amended) An integrated circuit (IC), comprising:

first and second input pins;

a first capacitor having a first end coupled to said first input pin and a second end;

a second capacitor having a first end coupled to said second input pin and a second end;

said first and second capacitors comprise first and second N-channel devices, respectively, each having its source and a drain coupled together at said first end and a gate forming said second end;

a first voltage divider coupled between DC sources and having a first junction coupled to said second end of said first capacitor;

a second voltage divider coupled between DC sources and having a second junction coupled to said second end of said second ~~capacitor; and~~capacitor;

a differential amplifier, having a differential input including a first input coupled to said first junction and a second input coupled to said second junction, and having an output that provides an output clock signal that is aligned with an input clock signal provided to at least one of said first and second input pins;

a third N-channel device having a source coupled to said source of said first N-channel device and a drain and gate coupled to said first junction; and

a fourth N-channel device having a source coupled to said source of said second N-channel device and a drain and gate coupled to said second junction.

11. (Original) The IC of claim 10, wherein said first input pin is selectively coupled to either a single-ended clock signal or a first polarity of a differential clock signal and wherein said second input pin is selectively disconnected or coupled to either one of a reference signal or a second polarity of said differential clock signal.

12. (Original) The IC of claim 10, further comprising multiple modes of operation including a first mode when said first input pin receives a single-ended clock signal and said second input pin is floated, a second mode when said first input pin receives a single-ended clock signal and said second input pin receives a reference signal, and a third mode when said first and second input pins receive first and second polarities of a differential clock signal.

13. (Cancelled)

14. (Cancelled)

15. (Currently Amended) The IC ~~of claim 14~~of claim 10, wherein said first and second voltage dividers each comprise:

a first P-channel device having a source and substrate coupled to a source voltage and a gate and a drain coupled to a corresponding one of said first and second junctions; and

a second P-channel device having a source and gate coupled to ground and a drain and a substrate coupled to a corresponding one of said first and second junctions.

16. (Original) The IC of claim 15, wherein said first and second N-channel devices are sized sufficiently large to overcome parasitic capacitances of said first and second P-channel devices of each of said first and second voltage dividers and wherein said third and fourth N-channel devices are relatively weak devices.

17. (Original) The IC of claim 15, wherein said differential amplifier comprises:

a fifth P-channel device having a source and a substrate coupled to a voltage source, a gate coupled to a center node and drain;

a sixth P-channel device having a source and a substrate coupled to said voltage source, and a gate and drain coupled together at said center node;

a fifth N-channel device having a source, a gate coupled to said first junction, and a drain coupled to said drain of said fifth P-channel device;

a sixth N-channel device having a drain coupled to said source of said fifth N-channel device, a gate coupled to said center node, and a source coupled to ground;

a seventh N-channel device having a source coupled to said source of said fifth N-channel device, a gate coupled to said second junction, and a drain coupled to said drain of said sixth P-channel device; and

an eighth N-channel device having a drain coupled to said source of said seventh N-channel device, a gate coupled to said center node, and a source coupled to ground.

18. (Original) The multiple mode clock receiver of claim 17, further comprising an inverter having an input coupled to said drain of said fifth P-channel device and an output providing an output clock signal.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)